



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/164,216	09/30/1998	RONALD PASQUALINI	NSC1-D8400	6392

7590

06/25/2002

MARK C. PICKERING
PILLSBURY WINTHROP LLP
50 FREMONT STREET, 5TH FLOOR
SAN FRANCISCO, CA 94105-2230

EXAMINER

NADAV, ORI

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 06/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application N .

09/164,216

Applicant(s)

PASQUALINI, RONALD 

Examiner

ori nadav

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 May 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 15, 19 and 38-56 is/are pending in the application.
- 4a) Of the above claim(s) 40-44 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 15, 19, 38, 39 and 45-56 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Art Unit: 2811

DETAILED ACTION

Election/Restriction

1. Applicant's election with traverse of the embodiment of figure 16 in Paper No. 21 is acknowledged. Applicant traverses withdrawing claims 40-44 from further consideration, because applicant argues that it is improper to restrict a dependent claim, because all the limitations of the independent claim are present in the dependent claim.

This is not found persuasive for the following reasons. The criteria for restricting dependent claims is not whether the limitations of the independent claim are present in the dependent claim. Dependent and independent claims can be restricted for being related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because diodes D1 and D2 (figure 1) can be used in the circuits of the embodiment of figure 16. The subcombination has separate utility such as diodes 800 and 1000 can be used in the circuit of figure 1. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of

Art Unit: 2811

their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 15, 19, 38-39 and 45-56 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. Figure 16 depicts positive lines being connected to pads via ESD switches. Claim 15 recites none of the positive lines being connected to a pad. Although the positive lines are not directly connected to the pads, there is no support for none of the positive lines being connected to pads, as recited in claim 15.

Art Unit: 2811

5. There is no support in the embodiment of figure 16 for the claimed limitations of a reverse breakdown voltage of a switch being less than the reverse breakdown voltage of the second diode, as recited in claim 51.

6. There is no support in the embodiment of figure 16 for the claimed limitations of ESD positive lines never being connected to a steady voltage source, as recited in claim 45.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 52 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitation of a positive line rises at a predetermined rate that is different from the predetermined rate, as recited in claim 52 is unclear as to what is it meant.

Art Unit: 2811

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 15, 19, 38-39 and 45-56, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al. (5,515,225) in view of Admitted Prior Art (APA).

Gens et al. teach in figure 2 a semiconductor chip having a substrate (figure 4, the external line encircling R1) of a first conductivity type, the chip comprising a plurality of pads P1, P2, an ESD negative ring R2, a plurality of ESD positive lines (the horizontal lines located between the high power supply terminals (the square blocks indicated as VDD1 and VDD2) and the line connecting the two diodes. See also column 3, lines 32-49) not being connected to a steady voltage source, not being electrically connected to each other and not encircling the periphery of the chip, a plurality of switches (diodes) connected between the ESD positive lines and the ESD negative ring, and a plurality of first and second diodes D1, D2 connected to a pad and the negative ring and positive line, respectively.

Although Gens et al. do not explicitly state that plurality of switches are connected between the ESD positive lines and the ESD negative ring, this feature is inherent in

Art Unit: 2811

Gens et al.'s device, because it is well known in the art that diodes are switches, of which official notice is taken. Therefore, Gens et al. teach plurality of switches being connected between the ESD positive lines and the ESD negative ring, as claimed.

Gens et al. do not teach plurality of positive lines not being connected to pads.

APA teaches in figures 1 and 2 a plurality of ESD switches including a transistor (figure 2) connected to the positive line and to the negative ring, respectively (page 2, lines 24-27), wherein the plurality of positive lines not being connected to pads

It would also have been obvious to a person of ordinary skill in the art at the time the invention was made not to connect the plurality of positive lines to the pads in Gens et al.'s device in order to provide more effective unidirectional flow of current during ESD operation.

Regarding claim 19, Gens et al. teach in figure 4 a negative line encircling the periphery of the chip.

Regarding claim 39, APA teaches in figure 2 a plurality of ESD switches including a transistor. It would also have been obvious to a person of ordinary skill in the art at the time the invention was made to use a transistor as an ESD switch in Gens et al.'s device, because it is well known in the art to use a transistor as an ESD switch, of which official notice is taken.

Art Unit: 2811

Regarding claim 46, Gens et al. teach in figure 2 a second diode having an anode electrically connected to a pad.

Regarding claim 51, APA teaches in figure 2 a reverse breakdown voltage of a switch 130 being less than the reverse breakdown voltage of the second diode.

Regarding claim 52, Gens et al. teach in figure 2 switches (diodes) blocking a current from flowing from the positive line to the negative ring.

Regarding claim 53, Gens et al. teach in figure 2 second diodes forward biased when the voltage on the positive lines rises at a predetermined rate.

Regarding claim 54, Gens et al. teach in figures 2 and 4 that none of the positive lines encircles the periphery of the chip.

Regarding claim 55, Gens et al. teach in figure 2 a positive line connected to a negative ring via a plurality of ESD switches.

Regarding claim 56, Gens et al. teach in figure 2 ESD switches (those connected to VDD1), not being connected to a pad P2.

Art Unit: 2811

Response to Arguments

11. Applicant argues on page 4 that ESD positive lines 1640-1647 are electrically isolated from each other, and figure 16 depicts that none of them is connected to a pad.

The examiner agrees that ESD positive lines 1640-1647 are electrically isolated from each other. However, figure 16 clearly depicts that ESD positive lines 1640-1647 are connected to a pad via diodes 1635. Thus, there is no support for none of the positive lines being connected to pads, as recited in claim 15.

12. Applicant argues on page 5 that the horizontal lines located between the high power supply terminals (the square blocks indicated as VDD1 and VDD2) and the line connecting the two diodes can not be read to be plurality of ESD positive lines, because Gens et al. categorize the square blocks VDD1 and VDD2 as power supply pads.

Although Gens et al. categorize the square blocks VDD1 and VDD2 as power supply pads, square blocks VDD1 and VDD2 provide positive power to the device. The positive power is provided to the diodes via the horizontal lines. Therefore, the horizontal lines are plurality of ESD positive lines, as claimed.

Art Unit: 2811

13. Applicant argues on pages 5-6 that Gens et al. do not teach the claimed limitation of claim 15, which recites that the positive lines are connected to the pads, because all blocks P1, P2, VDD1 and VDD2 are pads.

Claim 15 recites the limitation “none of the positive lines being connected to a pad”. Gens et al. teach in figure 2 positive lines (the lines connected to blocks VDD1 and VDD2) not being connected to a pad P2. Therefore, Gens et al. teach the claimed limitation of “none of the positive lines being connected to a pad”, as recited in claim 15.

14. Applicant argues on page 7 that Gens et al. and APA do not teach ESD positive lines never being connected to a steady voltage source.

There is no support in the embodiment of figure 16 for the claimed limitations of ESD positive lines never being connected to a steady voltage source, as recited in claim 45.

15. Applicant argues on pages 7-8 that Gens et al. do not teach a reverse breakdown voltage of a switch being less than the reverse breakdown voltage of the second diode, as recited in claim 51.

Art Unit: 2811

There is no support in the embodiment of figure 16 for the claimed limitations of a reverse breakdown voltage of a switch being less than the reverse breakdown voltage of the second diode, as recited in claim 51.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

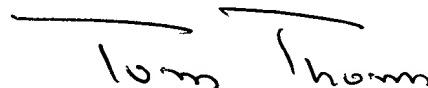
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art Unit: 2811

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**



TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Ori Nadav

June 20, 2002